Adaptive Compilation for a Reconfigurable, Object-Oriented Architecture

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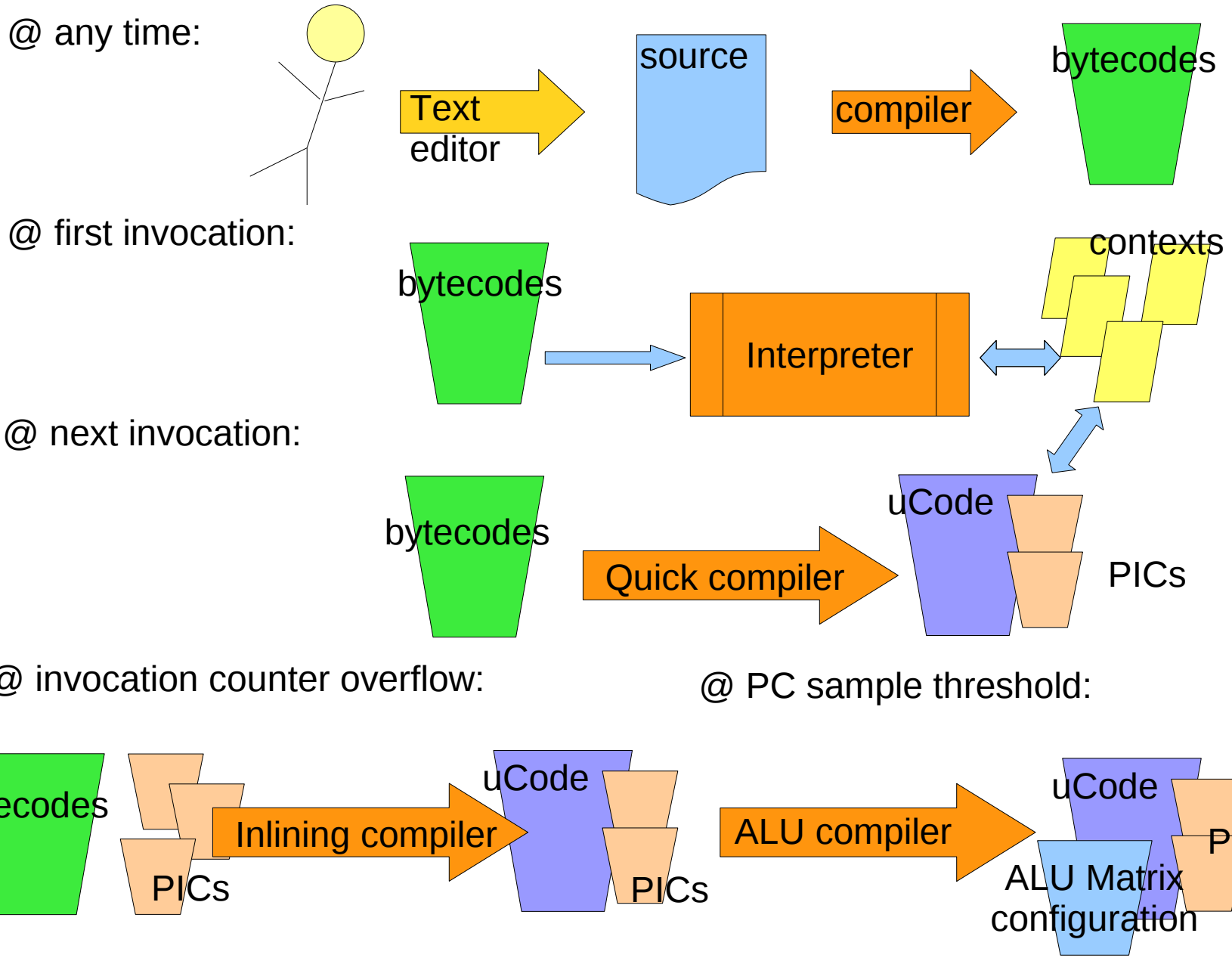
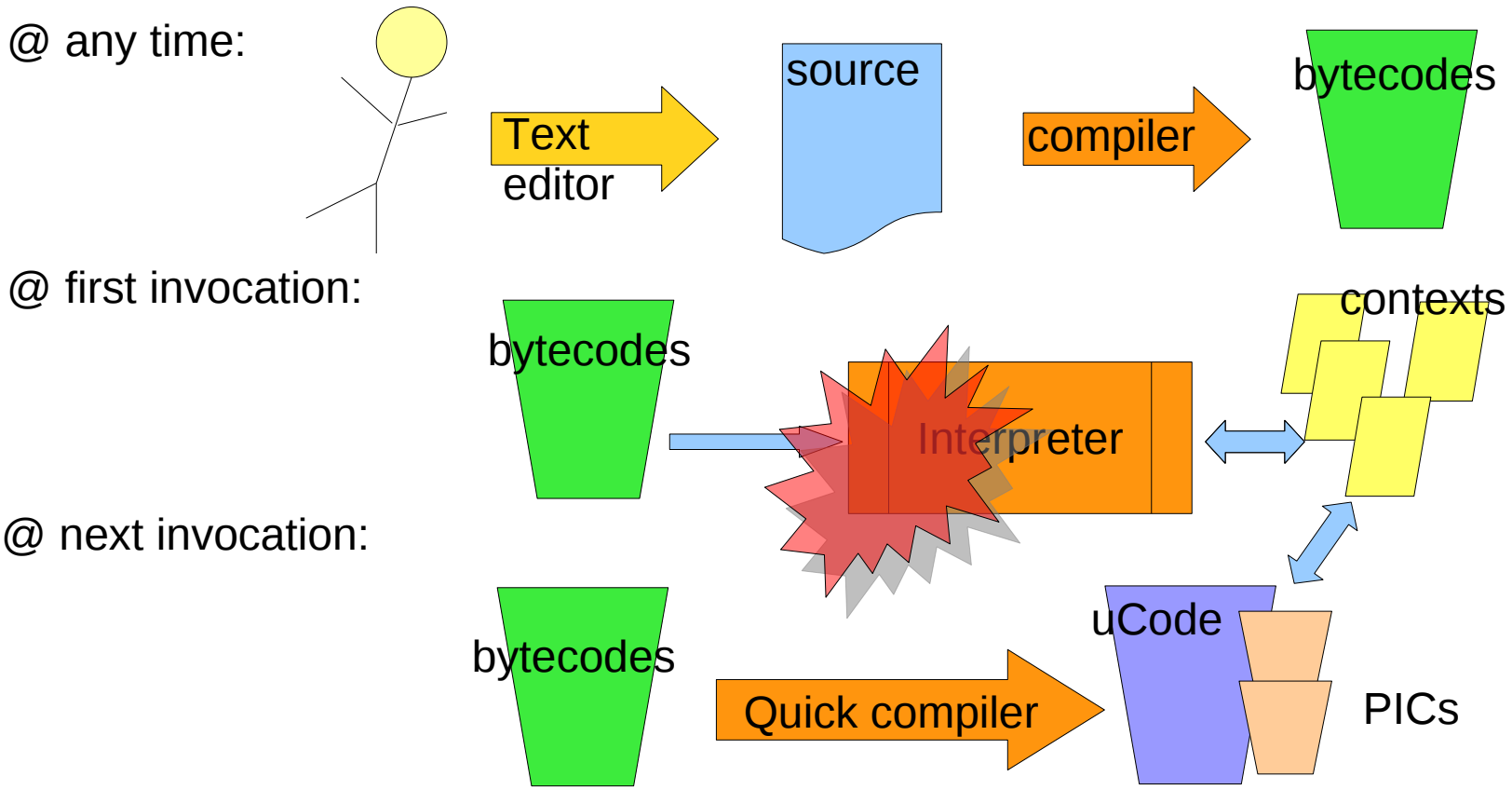
A method's life cycle

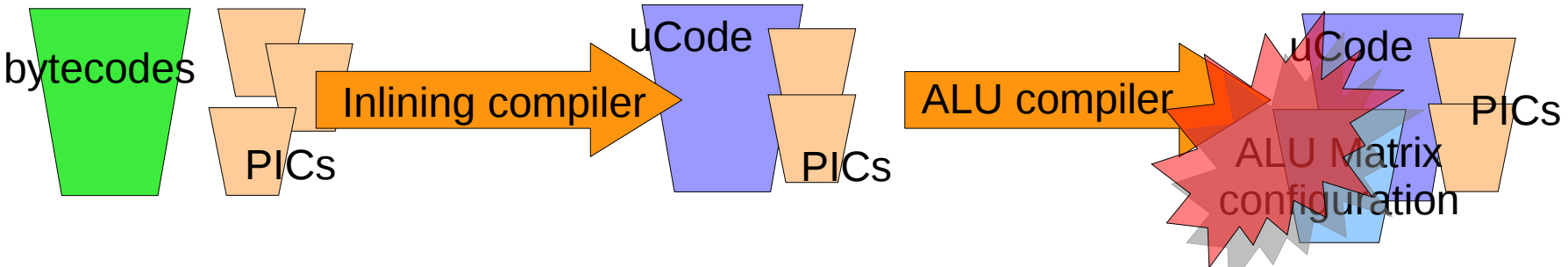


Reconfiguration (1 and 2)



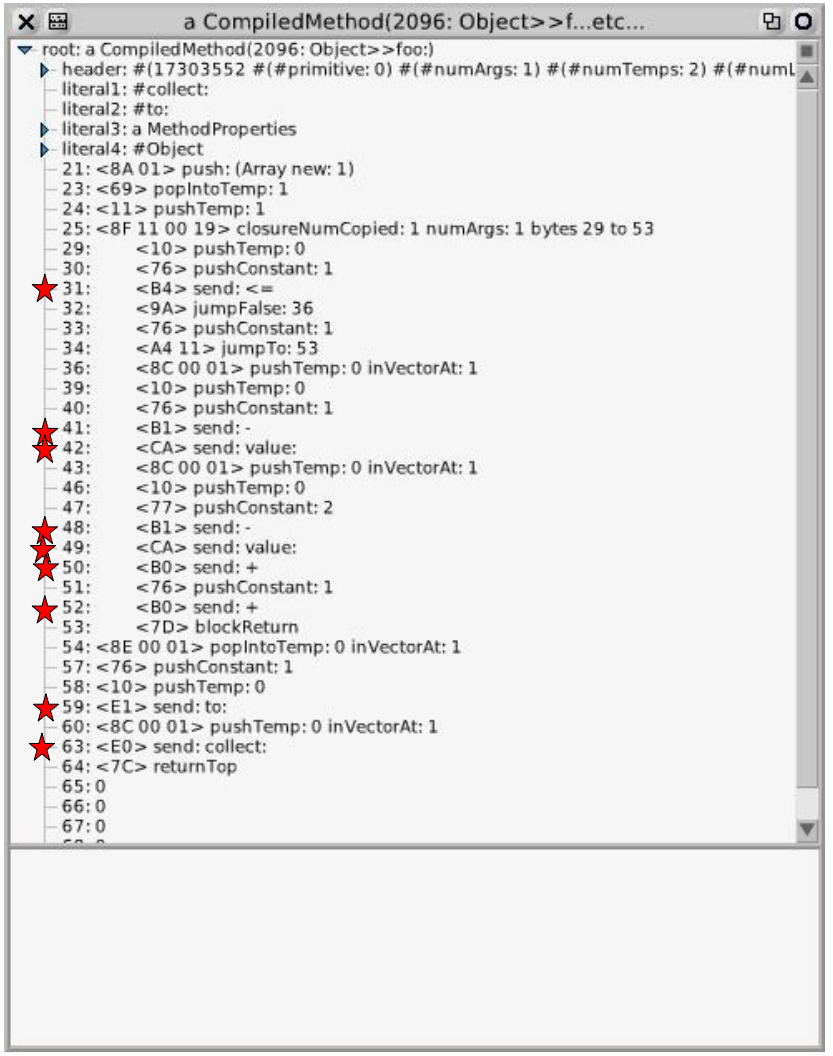
@ invocation counter overflow:

@ PC sample threshold:



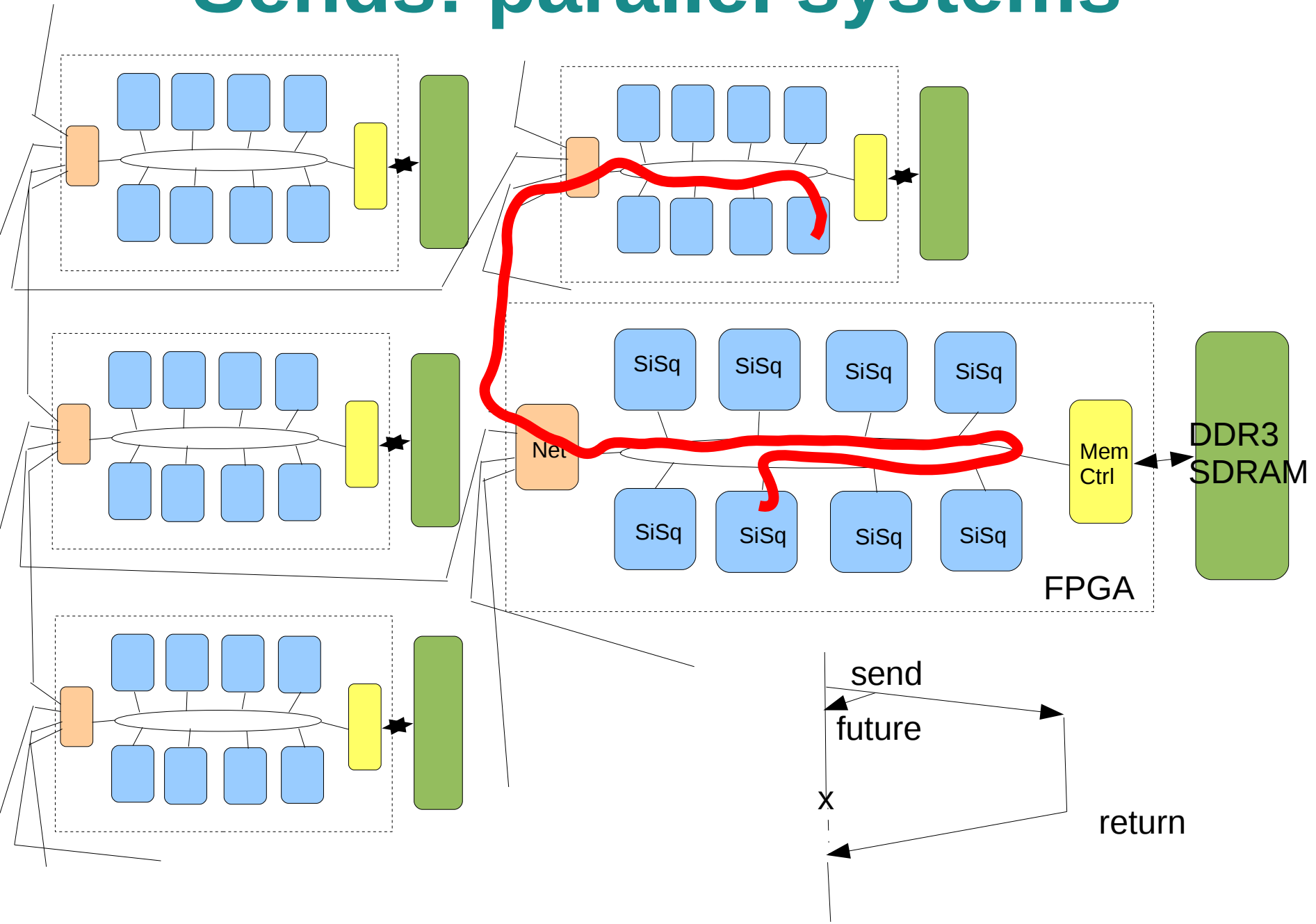
Bytecodes

```
foo: n
| nfib |
nfib := [:i | i <= 1 ifTrue: [1]
                    IfFalse: [(nfib value: i -1)
                                + (nfib value: i – 2)
                                + 1]].
^(1 to: n) collect: nfib
```

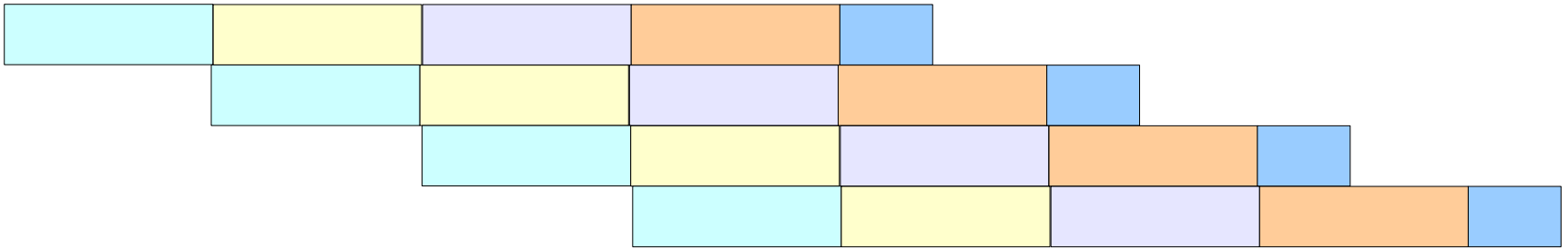


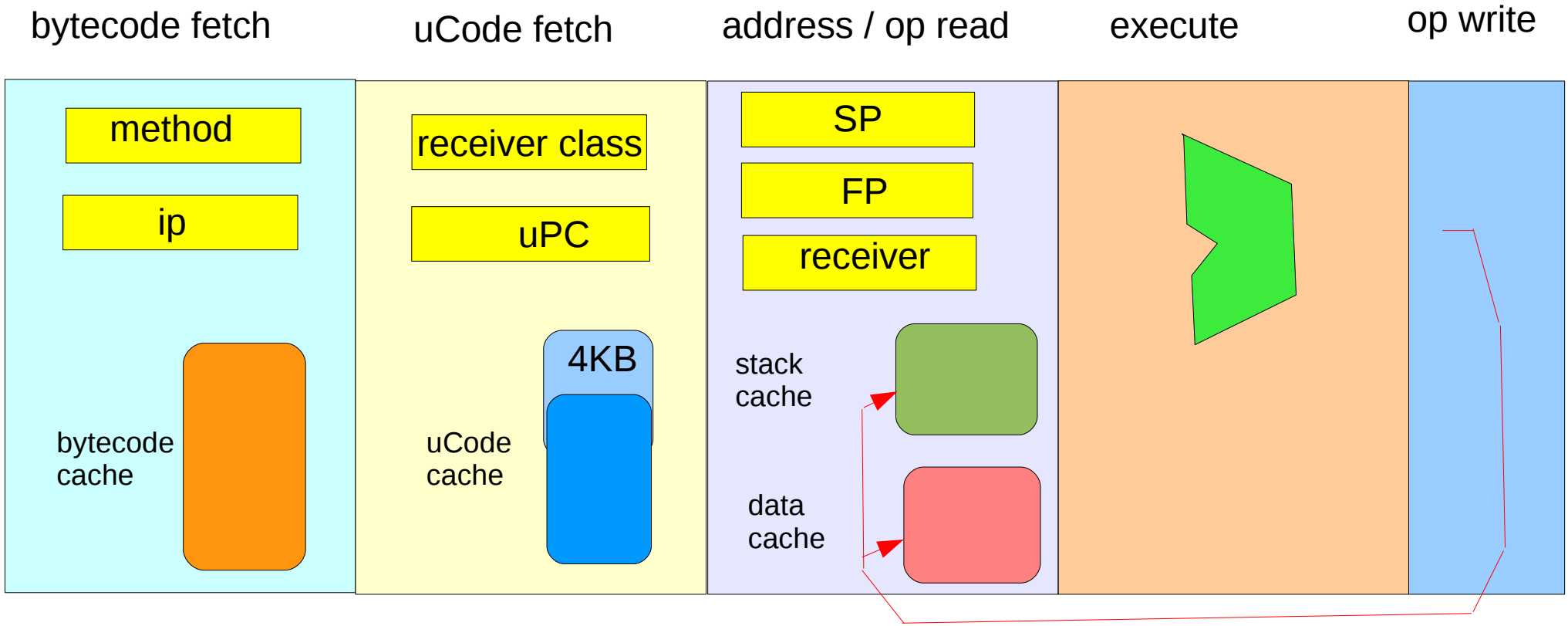
- ★ Indicates the send bytecodes

Sends: parallel systems

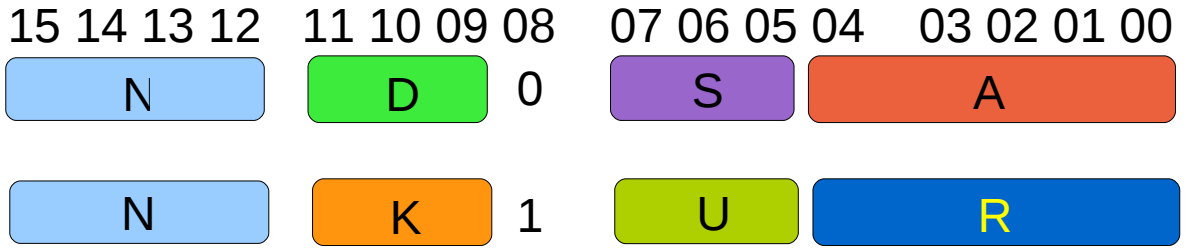


Interpreter





Microcode



N:
0000 next
0001 return
0010 skipOnZero
0011 skipOnOne
0100 PICuPC
0101 PIC2
0110 fetch8
0111 tagAndFetch8
1000 fetch1
1001 fetch2
1010 fetch3
1011 fetch4
1100 jump
1101 PICx
1110 call
1111 tagOrCall

K:
000 POP
001 STR
010 PSH
011 INR
100 ADR
101 SBR
110 ADK
111 SBK

U:
000 temporary
001 instance
010 stream
011 special
100 literal
101 immediate
11x ALU Matrix

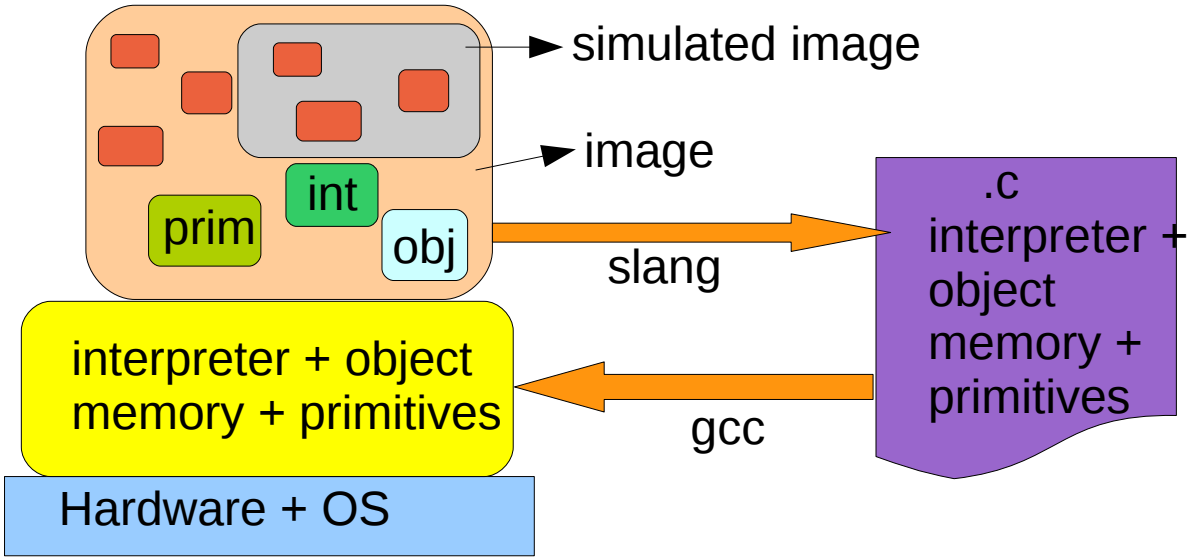
A:
00xxx - MOV, INC, NOT, NEG, ADD, ? , ? , SUB
01xxx - IOR, NOR, XOR, EQV, AND, ANI, NND, NAI
10xxx - SHR, SHL, ASR, ROT, MUL, DIV, UML, UDV
11xxx - EQL, CRY, MIN, OVF, LTN, LEQ, ULT, ULE

D or S = 111 means push or pop stack, while 000 to 110 indicate SP-0 to SP-6

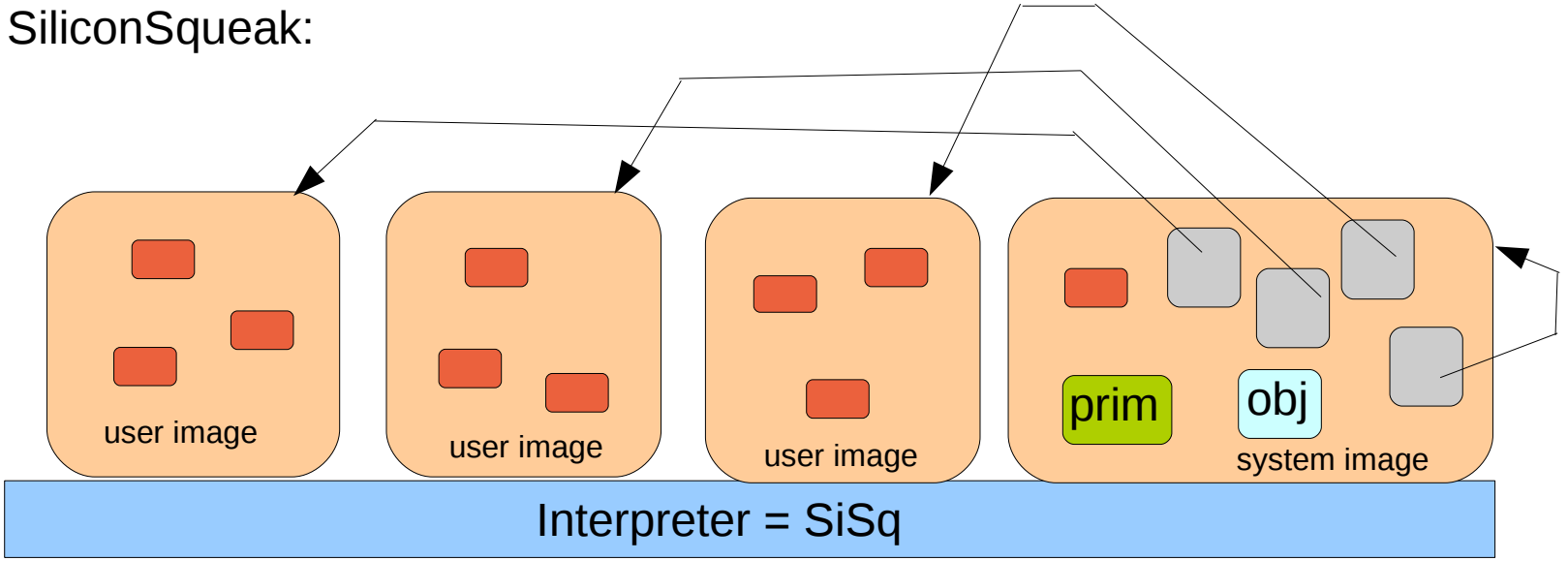
bit 15 = 1 means the 16 bits after the instruction are used to modify uPC

Memory and Primitives

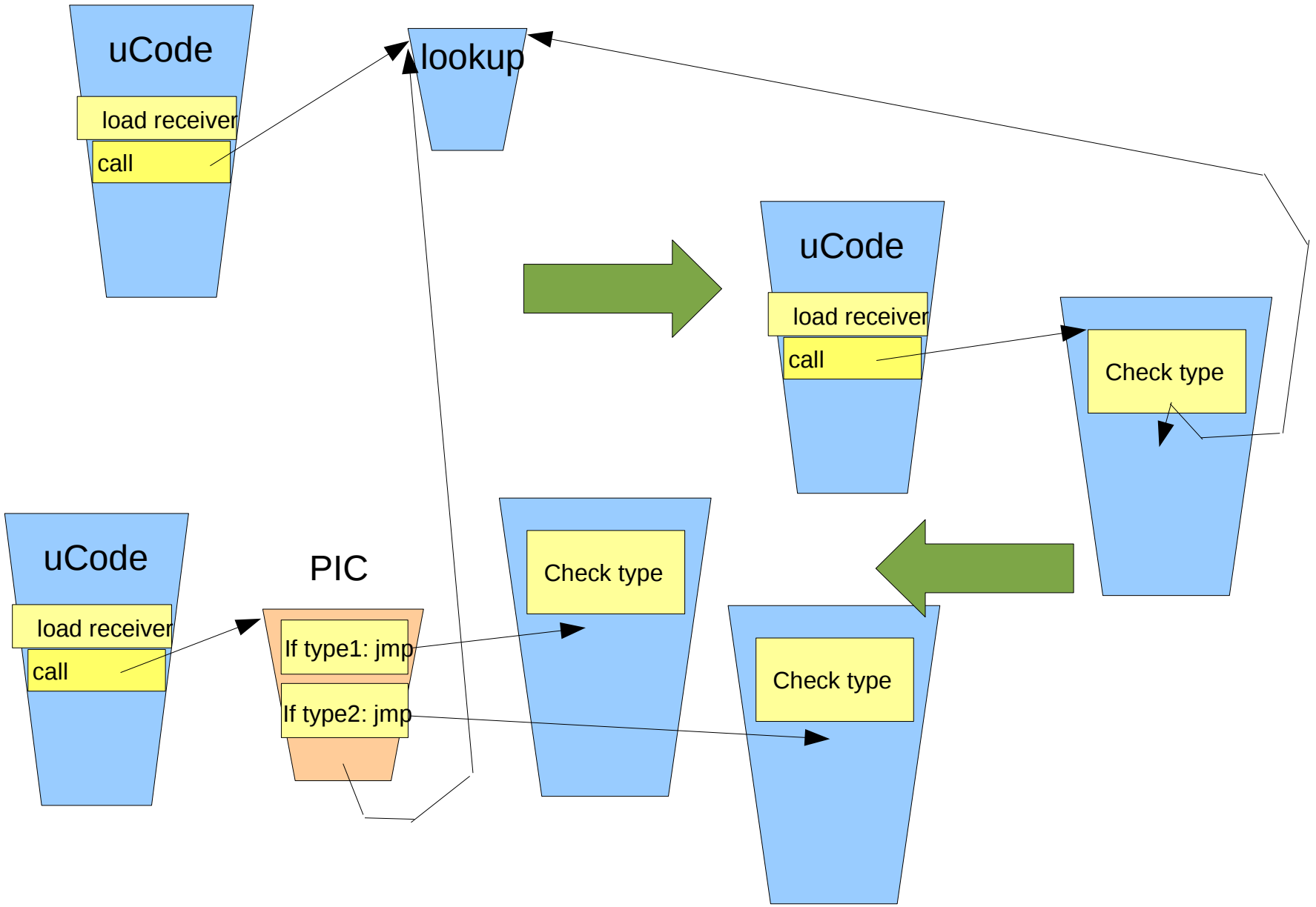
"Back to the Future":



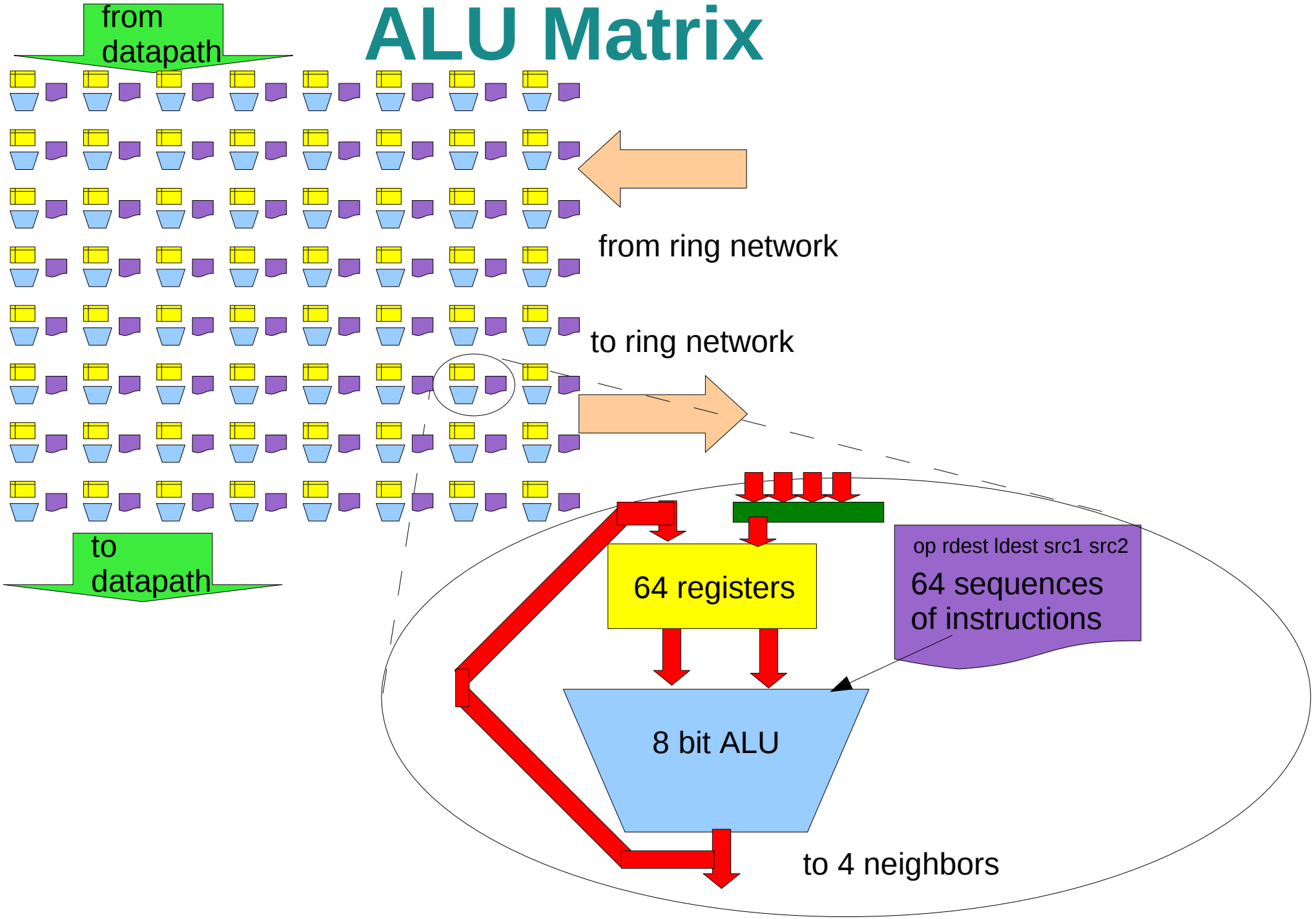
SiliconSqueak:



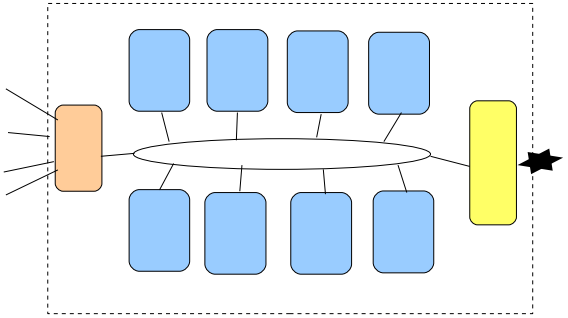
Polymorphic Inline Cache (PIC)

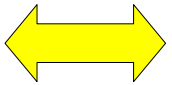


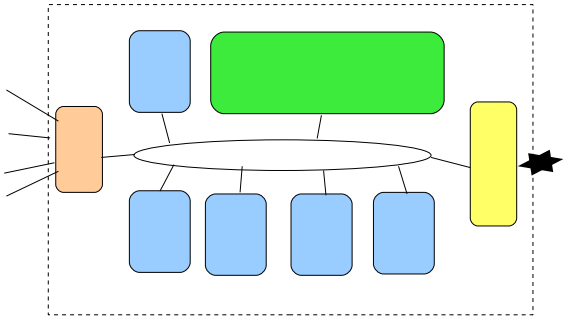
ALU Matrix

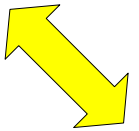

from datapath
from ring network
to ring network
to datapath
64 registers
op rdest ldest src1 src2
64 sequences of instructions
8 bit ALU
to 4 neighbors

Reconfiguration (3)



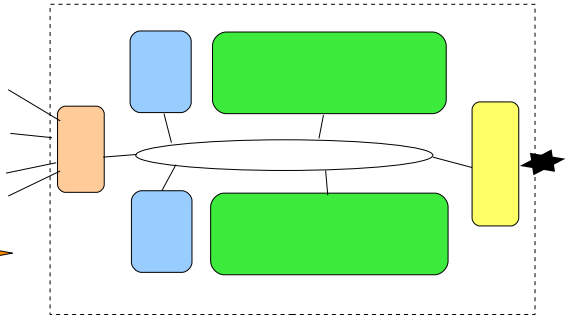






switch when:

1.4 x (time to reconfigure + time to execute in new configuration) <



time to execute in current configuration

Thanks!

- Parallelism
- Interpreter
- PICs
- ALU Matrix
- 3 types of Reconfiguration